brought to baseband. Chip-synchronized and frame-synchronized samples (real or complex) of the received signal (**64**) are stripped of a first component spreading sequence (**65, 66**). In one embodiment, the resulting signal is correlated simultaneously and in parallel with each of the possibly transmitted sequences (FIG. **2**). In another embodiment, the resulting signal is accumulated in a block of length equal to the common period of the sequences possibly transmitted (**67**) and is simultaneously correlated with all offsets of a second component sequence using transform techniques (**68**). In the preferred embodiment, the transforms are Hadamard transforms (FIG. **6**). The Hadamard transform is preceded by a permutation (**104**) of the input sequence. Alternatively, the transforms may be one-dimensional discrete Fourier Transforms implemented using, for example, a Fast Fourier Transform (FFT) algorithm (FIG. **4**), or a Winograd Fourier Transform Algorithm (WFTA) and cyclic convolution algorithms (FIG. **5**).

In a preferred embodiment, an informationless "pilot" sequence is transmitted in quadrature with the information bearing signal. Furthermore, information bearing signal can comprise a block error-correcting code (**150**). The block length of the block error correcting code (**150**) is equal to an integral multiple of the period of the pilot signal. The period of the pilot signal is an integral multiple of the information bearing signal. Thus, carrier recovery, sequence synchronization, and block code synchronization are all achieved simultaneously by correlating (synchronizing) the received signal with a baseband version of the pilot signal.

The present invention can be used in, for example, CDMA or mixed FDMA/TDMA/CDMA cellular communications or personal communication systems (PCS); spread spectrum over fiber channels; communications in license-free ISM bands; hybrid frequency-hopped and direct sequence spread spectrum tactical systems; traffic control; automatic toll taking; or any communications application that requires multipath rejection, interference tolerance, low interference to other users, robustness, and other advantages of direct sequence spread spectrum yet requires higher data rates and greater flexibility in data rates than normally provided by such systems.

The present invention is advantageous where bandwidth is limited (for example transmission over power lines, underwater, or other difficult channels), because increased data rate and processing gain can be achieved. The invention also provides flexibility in data rates; rapid synchronization enabling either synchronous or asynchronous operation; the ability to vary sequence length as well as power; and, enables threshold comparisons for detection of fades or loss of signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic illustration of a system for generating spreading sequences for use in a multiple sequence spread spectrum system.

FIG. **2** is a schematic illustration of a detection system for a spread spectrum signal in which the sender employs multiple spreading sequences for transmitting information where the number of candidate sequences is less than the number of stages in the generating registers.

FIG. **3** schematic illustration of a multiple-sequence spread spectrum receiver in which a block correlation method is used to simultaneously correlate a received signal with each possible candidate sequence.

FIG. **4** is a flow chart illustrating a block correlation method using fast Fourier transforms (FFTs) to correlate a received signal with each possible candidate sequence.

FIG. **5** is a flow chart illustrating a block correlation method using Winograd Fourier Transform Algorithms (WFTAs) and/or cyclic convolution algorithms to correlate a received signal with each possible candidate sequence.

FIG. **6** is a flow chart illustrating a block correlation method using fast Hadamard transforms (FHTs) to correlate a received signal with each possible candidate sequence.

FIG. **7** is a schematic illustration of a sequence generator in which an informationless, or pilot, signal is transmitted along with the information-bearing signal.

FIG. **8** is a schematic illustration of a carrier recovery and synchronization system for a signal that includes an information-bearing signal and an informationless, or pilot, signal.

FIG. **9** is a schematic illustration of a system in which forward error correction coding using a block code is combined with transmission of an informationless arm.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Sequence Generator

In FIG. **1**, a sequence generator for generating a multi-sequence spread-spectrum signal $\{s_k\}$ is shown. Information source **10** produces a sequence of information bits $\{i_k\}$. These bits are blocked into groups of $m \leqq n$ bits where 2^m is the number of sequences employed, and where n is the degree of polynomial $f_2(x) \epsilon GF(2)[x]$, whose non-zero coefficients correspond to the feedback taps of linear feedback shift register **14**. The degree of polynomial f_1 and f_2 is observed by counting the number of stages or slots from the center, (lowest slot on upper register **14** or highest slot of lower register **16**) to the last tap on register **14**, **16**. In FIG. **1**, both polynomials are of degree 5, however, polynomials f_1 and f_2 can be of different degree. In symbol selection unit **12**, each block of m bits is identified (via lookup table) with an n-bit "fill". A "fill" is a block of n bits that are "switched in" to the lower n bits of upper register **14** at the beginning of each symbol interval. Because arbitrary fills can be switched into the register, the number of sequences available to a user is limited only to 2^n (in FIG. **1**, 2^5=32). Consequently, 2^n fills and therefore a maximum of 2^n sequences are available and could be assigned to a single user.

The sequence generated by lower register **16** is arbitrary. Thus, it is not necessary that there be any relationship between the sequences propagating in the upper and lower registers. Indeed, in synchronous communications, only the sequence in the upper register need be periodic. The main purposes of the sequence in the lower register are to enable acquisition and maintenance of synchronism and detection of false synchrony and to enlarge the address space.

Sequences are assigned to a user by specifying (1) a pair of polynomials, (2) the number 2^m of sequences allocated to that user, and (3) an "initial fill"(the lower register can be assumed to contain the "impulse fill,"00 . . . 01). The initial fills corresponding to the 2^m sequences are the specified fill and the 2^m-1 fills that appear in the register as it is stepped 2^m-1 times, starting with the specified fill.

For example, suppose n=10 and all 1024 sequences of period 1023 are assigned to a single user, each sequence corresponding to a distinct initial fill of ten bits. This user can transmit eleven bits of information per symbol (1023 chips), ten bits corresponding to the sequence selected for